Applicants respectfully request reconsideration and allowance of the currently pending claims.

Allowable Subject Matter

Pending claim 12 has not been rejected or objected to by the Examiner. Applicants believe claim 12 to be allowable.

Drawings

The drawings are objected to because the Examiner contends that they do not show the features recited in claims 15-24, 26, and 30.

Claim 15 recites subject matter that is shown by example in Figs. 14 and 15. Fig. 15 has been corrected to show that bus 1216 provides inputs to XOR circuits 1204-1 to 1204-8. Specifically, claim 15 recites an apparatus comprising:

> a first circuit having a plurality of terminals;
> a first plurality of XOR circuits each having a first input coupled to one of the plurality of terminals, a second input coupled to receive a first periodic signal, and an output; and
> a second circuit having a first plurality of terminals each coupled to an output of one of the first plurality of XOR circuits, and a second plurality of terminals, wherein a number of the first plurality of terminals is different than a number of second plurality of terminals.

An example of the first circuit is shown as circuit 1202 of Fig. 14, where circuit 1202 connects to a bus 1216 that provides connection for the plurality of terminals of circuit 1202 as shown by lines A0 to A7 of Fig. 15.

An example of the first plurality of XOR circuits is shown in Fig. 15 as XOR circuits 1204-1 to 1204-8 that respectively couple to lines A0 to A7. The second input to XOR circuits 1204-1 to 1204-8 is from a periodic signal 1312 as shown in Fig. 15.

An example of the second circuit is shown as circuit 1306 in Fig. 15. As shown in Fig. 15, circuit 1306 has a plurality of terminals that couple to the outputs of XOR circuits 1204-1 to 1204-8. A second plurality of terminals of circuit 1306 is shown as lines 1308 and 1310 of Fig. 15.

Claim 16 recites a serializer, an example of which is shown as circuit 1306 in Fig. 15.

Claim 17 recites a shift register, an example of which is shown as elements 1302 and 1304 of Fig. 15.

Claim 18 recites a second plurality of XOR circuits, examples of which are shown as 1206-1 to 1206-8 in Fig. 15. A first input of each of the XOR circuits 1206-1 to 1206-8 is coupled to one of a plurality of terminals of circuit 1306, and an input of each of the XOR circuits 1206-1 to 1206-8 is coupled to receive the first periodic signal 1312 as shown in Fig. 15. The output of XOR circuits 1206-1 to 1206-8 is coupled to the first circuit by lines B0 to B7.

Claim 19 recites a deserializer, an example of which is shown as circuit 1306 of Fig. 15.

Claim 20 recites a shift register, an example of which is shown as elements1302 and 1304 of Fig. 15.

Claim 21 recites a second plurality of XOR circuits, and is illustrated by example in Fig. 14 by element1212 of Fig. 14 and by element 1212 of Fig. 15.

Claim 22 recites that the first inputs of the first plurality of XOR circuits are each coupled to the first circuit to receive first data in a first format at a first data rate of the first periodic signal, and the outputs of the first plurality of XOR circuits are structured to provide the first data in a second format to the second circuit. Claim 22 also recites that the first inputs of the second plurality of XOR

circuits are each coupled to the second circuit to receive the first data in the second format at a second data rate of the second periodic signal, and the outputs of the second plurality of XOR circuits are structured to output the first data in a third format. Examples of the first plurality of XOR circuits are represented by elements 1204-1 to 1204-8 of Fig. 15, and are described on page 24 line 20-22 of the present disclosure as reformatting the data patterns sent between circuits. Thus, elements 1204-1 to 1204-8 receive first data in a first format, and provide it in a second format to the second circuit. The second circuit 1306, in particular shift register 1302, receives the output of the first plurality of XOR circuits 1204-1 to 1204-8. The second circuit 1306, in particular shift register 1304, sends the output of the first plurality of XOR circuits 1204-1 to 1204-8 to the second plurality of XOR circuits 1206-1 to 1206-8. The second plurality of XOR circuits 1206-1 to 1206-8 in turn outputs this data in a third format. This is described on page 26 lines 4-19 of the present disclosure.

Claim 23 further recites that the first data rate of the first periodic signal is an integer multiple of the second data rate of the second periodic signal. The least significant address bit A0 can be used on line 1314 the second periodic signal, and address bit A3 can be used as the first periodic signal 1312. A3 is an integer multiple of A0. See page 26 lines 9-14 of the present disclosure.

Claim 24 further recites that the first circuit comprises a memory for storing the first data, that the first periodic signal comprises a first address signal for addressing the memory, and that the second periodic comprises a second address signal for addressing the memory. Fig. 10 illustrates a memory 804 that stores the first data. The use of particular address bits for the first and second periodic signals is described on page 19 line 19 to page 20 line 1.

Claim 26 recites a second circuit for storing the first predetermined number. The second circuit is shown as circuit 802 with a memory 804 for storing the first predetermined number, as shown in Fig. 13.

Claim 30 recites that the second device further comprises a third plurality of XOR circuits having first inputs to receive second data, second inputs each coupled to receive a bit of a second predetermined number, and outputs. In Fig. 13, the third plurality of XOR circuits is represented by 812. As discussed in the specification (see pg. 24 line 16 – pg. 26 line 19 of present disclosure), an XOR circuit may comprise of multiple XOR circuits for multiple bit values). XOR circuit 812 receives second data from memory 804. Input 855 has a second predetermined number and is an input to the second input of XOR circuit 812.

Claim 30 further recites the first device further comprises a fourth plurality of XOR circuits having first inputs coupled to the outputs of the third plurality of XOR circuits, second inputs each coupled to receive a bit of the second predetermined number, and outputs coupled to the first circuit. As illustrated in Fig. 13, the first device 1102 comprises a fourth XOR circuit 1108 having an input coupled to data bus 818, where data bus 818 is coupled to output of XOR circuit 812. An input of XOR circuit 1108 is coupled to input 855 having the second predetermined number. The output of XOR circuit 1108 is received at a first circuit shown as control logic 1106.

As summarized above, examples of the elements recited in claims 15-24, 26, and 30 are shown in Figs. 13, 14 and 15. Thus, it is believed that the drawing objection under 37 CFR 1.83(a) is improper, and should be withdrawn.

35 U.S.C. §112

Claims 8, 15-24, 26, and 30 are rejected as under §112, second paragraph.

Claim 8 has been rejected as having no antecedent basis for first data of line 2. The word "data" is the plural form of the singular "datum" and therefore it would be grammatically incorrect to claim "first data" as "a first data."

Claim 15 describes "second circuit having ... a second plurality of terminals." This defines the "connective relationship" of the second plurality of terminals.

Claims 16-24, 26 and 30 have been discussed above as to Figs. 14 and 15 showing the features specified by the claims.

35 U.S.C. §103

Claims 8-11, 13-14, and 39-47 are rejected under 35 U.S.C § 103 as being unpatentable over U.S. Patent 5,680,354 by Kawagoe (Kawagoe), in view of U.S. Patent 5,881,019 to Koshikawa (Koshikawa).

Independent claim 8 recites "a first XOR circuit having a first input to receive first data in a first format, a second input to receive a periodic signal other than the first data; and an output to provide the first data in a second format; and a second XOR circuit having a first input coupled to the output of the first XOR circuit, a second input coupled to receive the periodic signal other than the first data, and an output to provide the first data in the first format."

Kawagoe does not suggest or teach that either of the first or second XOR circuits receives a periodic signal as an input. The Office Action concludes that signal S2 of Kawagoe's Fig. 1 is a "periodic address signal." However, this conclusion is incorrect. At col. 6, lines 37-42, Kawagoe states:

> A defective bit address registering circuit 4 registers an address of a bit line to which a defective memory cell is connected, and outputs an output signal S2 at an "H" level if address buffer output signals A0, . . . , An, /A0, . . . , /An match a registered address.

Thus, Kawagoe's "circuit 4" receives addresses, compares them to addresses of defective cells, and outputs a true signal at S2 if a particular address corresponds to a defective cell. Signal S2 therefore has a random timing, depending on the locations or addresses of defective cells. Being random, S2 cannot be considered periodic.

Signal S2, although generated in partial response to an address signal, is not itself an address signal or address bit. Furthermore, there is nothing in the Kawagoe reference suggesting that S2 would be periodic. To the contrary, it appears that S2 would have a random timing, dependent on the locations or addresses of defective cells.

Thus, the XOR circuits of Kawagoe's Fig. 1 do not receive a periodic signal as argued by the Examiner. Since claim 8 recites that inputs of the first and second XOR circuits receive a periodic signal, and since Kawagoe does not show or suggest such an arrangement, claim 8 the rejection of claim 8 is unsupported by the prior art.

Koshikawa is cited only in relation to the burst counter recited in claim 11, and not to show an XOR circuit that receives a periodic signal. Accordingly, neither Kawagoe nor Koshikawa suggests the particular configuration recited in claim 8.

Applicants respectfully request that the §103 rejection of claim 8 be withdrawn.

Dependent claims 9-14 are allowable by virtue of their dependency on base claim 8 and because of the additional elements recited therein. For

example, claim 10 further recites that "the periodic signal comprises an address signal for addressing the memory." As discussed above, the signal S2 described in Kawagoe is not an address bit or an address signal. Koshikawa is cited for teaching a burst counter, however, does not suggest or teach a periodic signal that comprises an address signal.

Claim 11, which depends from claim 10, further recites "wherein the address signal is generated by a burst counter." As discussed, the signal S2 described in Kawagoe is not an address signal. Koshikawa is cited for teaching a burst counter, however, a combination of Kawagoe and Koshikawa does not suggest or teach that a burst counter may generate an address signal to be used as an input since Kawagoe does not teach that the input is an address signal.

Applicants respectfully request that the §103 rejection of claims 9-14 be withdrawn.

Independent claim 39 recites "writing data to the memory device via a first XOR circuit clocked by a periodic signal other than a data signal." As discussed, Kawagoe does not suggest nor teach the use of a period signal to clock an XOR circuit. Koshikawa is cited for teaching a burst counter, however, does not suggest or teach the use of periodic signal as an input to an XOR circuit.

Applicants respectfully request that the §103 rejection of claim 39 be withdrawn.

Independent claim 40 recites "writing data to the memory device via first XOR circuit clocked by a periodic signal other than the data; and reading the data from the memory device via a second XOR circuit clocked by the periodic signal." As discussed Kawagoe does not suggest or teach the use of a periodic signal to clock an XOR circuit.

Applicants respectfully request that the §103 rejection of claim 40 be withdrawn.

Independent claim 41 recites "accessing a memory device comprising: providing first data to a bus interface of the memory device in a first format and at a first data rate; reformatting the first data to a second format in response to an address signal, the second format having a second data rate different than the first data rate; and storing the first data in the memory device in the second format."

Although the Examiner has rejected claim 41 based on a combination of Kawagoe and Koshikawa, the Examiner has not addressed the elements of claim 41 in regards to Kawagoe and Koshikawa. In particular, the Examiner has not shown how a combination of Kawagoe and Koshikawa would suggest or teach providing a first data at a first data rate and reformatting the first data to a second format in response to an address signal to, where the second format has a second data rate different than the first data. Fig. 1 of Kawagoe shows a memory device 1 that receives data. Kawagoe, however, does not suggest or teach reformatting this data to a second format having a different data rate in responses to an address signal. Koshikawa is cited for teaching a burst counter, however, does not suggest or teach reformatting data to a second format having a different data rate.

Accordingly, applicants respectfully request that the §103 rejection of claim 41 be withdrawn.

Dependent claims 42 and 43 are allowable by virtue of their dependency on base claim 41, and by virtue of the additional elements recited therein. Applicants respectfully request that the §103 rejection of claims 42 and 43 be withdrawn.

Independent claim 44 recites "a reformatting circuit receiving data in a first format at a first data rate from the data bus, and reformatting the data to a second format in response to an address signal on the address bus that alternates the first data rate, the reformatted data having a second data rate that is different than the first data rate; and a memory circuit coupled to the reformatting circuit and storing the reformatted data."

The Examiner has rejected claim 44 based on a combination of Kawagoe and Koshikawa; however, the Examiner has not addressed the elements of claim 41 in regards to Kawagoe and Koshikawa. As discussed above in relation to the allowabilitly of claim 41, the Examiner has not dealt with the particular elements regarding reformatting a data having a first data rate to a reformatted data having a second data rate. Kawagoe nor Koshikawa suggest or teach the use of different data rates.

Applicants respectfully request that the §103 rejection of claim 44 be withdrawn.

Dependent claims 45-47 are allowable by virtue of their dependency on base claim 44 and by virtue of the additional elements recited therein. Applicants respectfully request that the §103 rejection of claims 45-47 be withdrawn.

Claims 15-36 are rejected under 35 U.S.C § 103 as being unpatentable over U.S. Patent 5,295,188 by Wilson et al (Wilson), in view of U.S. Patent 4,071,889 to Sumida et al (Sumida).

Independent claim 15 recites "a first circuit having a plurality of terminals; a first plurality of XOR circuits each having a first input coupled to one of the plurality of terminals, a second input coupled to receive a first periodic signal, and an output; and a second circuit having a first plurality of terminals each

coupled to an output of one of the first plurality of XOR circuits, and a second plurality of terminals, wherein a number of the first plurality of terminals is different than a number of second plurality of terminals."

Wilson does not suggest or teach that first XOR circuits receive a periodic signal as an input. Furthermore, the Examiner has not pointed out the existence of any periodic signals in the relevant portions or Figures of Wilson or Sumida, and in particular has not pointed out any XOR circuits that receive periodic signals.

Wilson describes a "decoder 68 gates logic states of the selected row ... to one input of XOR gates 74." Wilson at col 13 lines 61-63. Wilson also describes that "[t]he other inputs to XOR gates 74 are provided via bus 76 by the remainder of the memory locations of buffer 56 and consist of the six least significant bits of the first intermediate block." Wilson at col. 14 lines 10-13.

Wilson's logic states that are described as an input to XOR gates 74, and the other inputs to XOR gates 74 depend on a matrix T created by T Matrix Generator 63 which are shown in Fig. 3 of Wilson. Wilson describes that "a public key K is formed by the multiplication of a pair of private key binary matrices, designated as matrix T and M." Wilson at col.5 lines 44-47. The matrix T is a value which is dependent on a randomly determined public key K. Therefore the outputs and the inputs to XOR gates, from matrix T are not periodic, but are randomly dependent on the matrix T that is generated by T Matrix Generator 63. Thus the XOR gates of Wilson's Fig. 3 do not receive a periodic signal.

Sumida is cited only in relation to the shift register of claim 17 and not to show XOR circuits that receive a periodic signal. Accordingly, neither Wilson nor Sumida suggests the particular configuration recited in claim 15.

Applicants respectfully request that the §103 rejection of claim 15 be withdrawn.

Dependent claims 16-20 are allowable by virtue of their dependency on base claim 15 and by virtue of the additional elements recited therein.

Applicants respectfully request that the §103 rejection of claims 16-20 be withdrawn.

Independent claim 25 recites "a first device comprising: a first circuit; a first plurality of XOR circuits having first inputs coupled to receive first data from the first circuit, second inputs each coupled to receive a bit of a first predetermined number, and outputs; and a second device comprising: a second plurality of XOR circuits having first inputs coupled to the outputs of the first plurality of XOR circuits, and second inputs coupled to receive one bit of the first predetermined number."

The signals received by XOR circuits 74 are dependent on words representing noise, meaning that the words and their bits can change. (See Wilson at col. 13 line 61 to col. 14 line 28). The Examiner equates XOR circuits 84 of Wilson's Fig. 3 to a second plurality of XOR circuits. The first inputs of XOR circuits 84 receive an output of XOR circuits 74; however, the second inputs of XOR circuits 84 are the "four least significant bits of the third row of the second fourlet." (See Wilson col. 14 lines 16-28). The bit data of the second inputs of XOR circuits 84 originate from a different source (third row of second fourlet) than either the inputs to XOR circuits 74 (logic state information and buffer memory information). Wilson does not suggest nor teach "a first plurality of XOR circuits having ... second inputs each coupled to receive a bit of a first predetermined number ...and ... a second plurality of XOR circuits having ...

second inputs coupled to receive one bit of the first predetermined number." The inputs to XOR circuits 74 are from logic state information and buffer memory information, and the inputs to XOR circuits 84 are from the output of XOR circuits 74 and from the third row of the second fourlet.

Sumida is cited only in relation to the shift register that is not recited in claim 25 or independent claims 26-32, and not to show XOR circuits that receive a a bit of a predetermined number. Accordingly, neither Wilson nor Sumida suggests the particular configuration recited in claim 25.

Applicants respectfully request that the §103 rejection of claim 25 be withdrawn.

Dependent claims 26-32 are allowable by virtue of their dependency on base claim 25 and by virtue of the additional elements recited therein. Applicants respectfully request that the §103 rejection of claim 25 be withdrawn.

Amended independent claim 34 recites in part "a first plurality of XOR circuits having ... second inputs each coupled to receive a bit of a predetermined number ... and a second plurality of XOR circuits having ... second inputs coupled to the predetermined number."

As discussed above, Wilson discloses inputs to XOR circuits 74 are from logic state information and buffer memory information, and inputs to XOR circuits 84 are from the output of XOR circuits 74 and from the third row of the second fourlet.

Sumida is cited only in relation to the shift register and not to show XOR circuits that receive a a bit of a predetermined number. Accordingly, neither Wilson nor Sumida suggests the particular configuration recited in claim 34.

Applicants respectfully request that the §103 rejection of claim 33 be withdrawn.

Dependent claims 35-36 are allowable by virtue of their dependency on base claim 33 and by virtue of the additional elements recited therein. Therefore, it is respectfully requested that these claims be allowd.

Conclusion

All pending claims 8-26, 29-32, 34-36, and 39-47 are in condition for allowance. Applicants respectfully request reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Dated: 1/29/03

By: _____

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MARKED UP VERSION OF PENDING CLAIMS UNDER 37 C.F.R. § 1.121(C)(1)(ii):

Amend claim 34-36, 39 as follows and in accordance with 37 C.F.R. § 1.121(c)(1)(ii), by which the Applicant submits the following marked up version only for claims being changed by the current amendment, wherein the markings are shown by brackets (for deleted matter) and/or underlining (for added matter):

34. (Once Amended) An[The] apparatus[of claim 33, further] comprising:

a first circuit;

a first plurality of XOR circuits having first inputs coupled to receive first data from the first circuit, second inputs each coupled to receive a bit of a predetermined number;

a second circuit providing the first predetermined number to the first plurality of XOR circuits; and

a second plurality of XOR circuits having first inputs coupled to outputs of the first plurality of XOR circuits, second inputs coupled to the predetermined number, and outputs coupled to the first circuit.

35. (Once Amended) The apparatus of claim 3[3]4, wherein the predetermined number is only one bit.

36. (Once Amended) The apparatus of claim 3[3]4, wherein the second circuit comprises a pseudo-random number generator.

39. (Once Amended) A method of accessing a memory device comprising:

writing data to the memory device via a first XOR circuit clocked by a periodic signal other than [the]a [first] data signal.

MARKED UP VERSION OF SPECIFICATION UNDER 37 C.F.R. § 1.121(B)(1)(iii):

Page 23, fourth paragraph

For one embodiment, address bit A_0 is also used to generate the ALT signal on line 855 and 1118 that is applied as an input to XOR gates 810, 812, 1108, and 1110. For one embodiment, the address rate on lines 853 and 1118 is the same rate as the dat[e]a rate on lines 818. The address bit A_0 toggles at the maximum rate of the addresses and thus functions also as the ALT signal for the reformatting circuitry.